GaAs Dual-Gate FET for Operation up to *K*-Band

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Abstract — **A high-frequency equivalent circuit model of a GaAs dual-gate FET and analytical expressions for the input/output impedances, transconductance, unilateral gain, and stability factor are presented in this paper. It is found that the gain of a dual-gate FET is higher than that of a single-gate FET at low frequency, but it decreases faster as frequency increases because of the capacitive shunting effect of the second gate. A dual-gate power FET suitable for variable gain amplifier applications up to *K*-band has been developed. At 10 GHz, a 1.2-mm gatewidth device has achieved an output power of 1.1 W with 10.5-dB gain and 31-percent power-added efficiency. At 20 GHz, the same device delivered an output power of 340 mW with 5.3-dB gain. At *K*-band, a dynamic gain control range of up to 45 dB was obtained with an insertion phase change of no more than ±2 degrees for the first 10 dB of gain control.**

I. Introduction

EVER SINCE ITS inception in 1971, the GaAs dual-gate MESFET has found increasing areas of applications. Variable gain amplification [1], active phase shifting [2], mixing [3], UHF tuning [4], and pulse reshaping [5] are making use of the second gate to perform these specific functions. Papers dealing mostly with the low-frequency aspects of dual-gate FET models have appeared in many of the scientific journals [6]–[8]. Increased understanding of the dual-gate FET operation will undoubtedly lead to a more optimized structure for a particular application. Few papers, however, have addressed the important issues of high-frequency device modeling and power operation [9], [10]. It is the intention of this paper to derive an analytical model for explaining the high-frequency performance of a dual-gate FET [11]. This study has led to the development of a GaAs dual-gate power FET suitable for applications up to *K*-band [12].

II. High-Frequency Equivalent Circuit

A commonly used dual-gate FET model is shown in Fig. 1. It is a cascode connection of two FET's, one common-source and one common-gate configuration with a coupling capacitor C_f between them [6]. In a simplified equivalent circuit, the input impedance is the same as that of a comparable single-gate FET, but the output impedance is quite different. The output resistance R_{out} and the transconductance G_{md} of a dual-gate FET at low frequencies are given by [7]

$$G_{md} \simeq g_{m1} \tag{1a}$$

$$R_{\text{out}} \simeq R_{ds1} R_{ds2} g_{m2} \tag{1b}$$

where g_m's are transconductances and R_{ds}'s are output resistances, while subscripts 1 and 2 represent the values associated with the first and the second FET's. Due to the large output resistance, the unilateral gain of the dual-gate FET is $R_{ds1} \cdot g_{m2}$ times higher than that of a comparable single-gate device. However, at high frequencies, the device behaves quite differently.

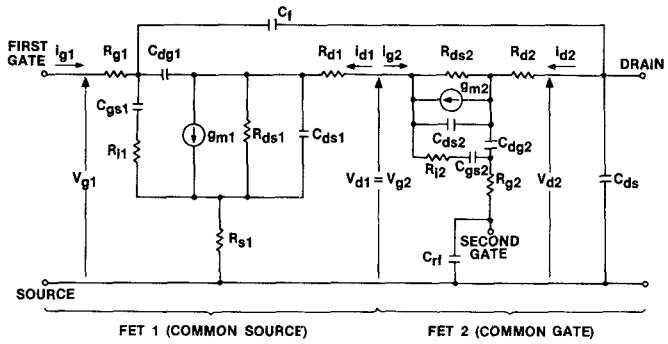

Fig. 1. Equivalent circuit of a GaAs dual-gate FET.

The Y matrices of the two component FET's are defined by

$$\begin{aligned} i_{g1} &= Y_{g1} v_{g1} + Y_{mg1} v_{d1} \\ i_{d1} &= Y_{md1} v_{g1} + Y_{d1} v_{d1} \end{aligned} \tag{2a}$$

$$\begin{aligned} i_{g2} &= Y_{g2} v_{g2} + Y_{mg2} v_{d2} \\ i_{d2} &= Y_{md2} v_{g2} + Y_{d2} v_{d2} \end{aligned} \tag{2b}$$

where i represents current, v represents voltage, subscripts g and d represent gate and drain values, and subscripts 1 and 2 represent the first and the second FET's, respectively.

The Y matrices of the overall dual-gate FET are defined by

$$\begin{aligned} i_{g1} &= Y_{11} v_{g1} + Y_{12} v_{d2} \\ i_{d2} &= Y_{21} v_{g1} + Y_{22} v_{d2}. \end{aligned} \tag{3}$$

The parameters of the Y matrices of the FET's are derived and are summarized in Table I. In the derivation, it is assumed that the output impedance of the first FET is

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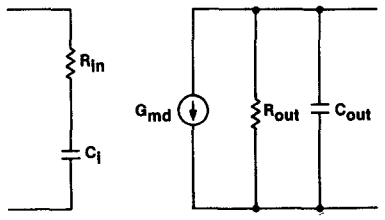

Fig. 2. (a) Input and (b) output equivalent circuits of a dual-gate FET.

TABLE I
Y MATRIX PARAMETERS OF DUAL-GATE FET

	FIRST FET	SECOND FET	OVERALL FET
$Y_g(Y_{11})$	$1/(Z_{in1}-jR_{s1}B_1)$	$(1-jB_2)/Z_{in2}$	$Y_{g1}-\frac{Y_{mg1}Y_{md1}}{Y_{d1}+Y_{g2}}+j\omega C_f$
$Y_d(Y_{22})$	$(j\omega C_{dg1}+Z_{in1})/\lvert Z_{out1}(Z_{in1}-jR_{s1}B_1)\rvert$	$j\omega C_{dg1}+1/Z_{out2}+\omega C_{dg1}\frac{B_2 Z_{rf}}{Z_{in2}}+j\omega C_{ds}$	$-\frac{Y_{md2}Y_{mg2}}{Y_{d1}+Y_{g2}}+Y_{d2}+j\omega C_f$
$Y_{mg}(Y_{12})$	$-j\omega C_{dg1}-R_{s1}Y_{g1}/Z_{out1}$	$-\frac{1}{Z_{out2}}-\frac{Z_{rf}(1-jB_2)j\omega C_{dg1}}{Z_{in2}}$	$-\frac{Y_{mg1}Y_{mg2}}{Y_{d1}+Y_{g2}}-j\omega C_f$
$Y_{md}(Y_{21})$	$-jB_1 Y_{g1}$	jB_2/Z_{in2}	$-\frac{Y_{md1}Y_{md2}}{Y_{d1}+Y_{g2}}-j\omega C_f$

* SYMBOLS ARE DEFINED AS FOLLOWS:

$Z_{in1}=R_{i1}+R_{g1}+R_{s1}+1/j\omega C_{gs1}$	$Z_{in2}=R_{i2}+Z_{rf}+1/j\omega C_{gs2}+R_{g2}$	$Z_{rf}=\frac{1}{j\omega C_{rf}}$
$Z_{out1}=1/(j\omega C_{ds1}+1/R_{ds1})$	$Z_{out2}=1/(j\omega C_{ds2}+1/R_{ds2})$	$f_{T1}=\frac{g_{m1}}{2\pi C_{gs1}}$
$B_1=f_{T1}/f$	$B_2=f_{T2}/f$	$f_{T2}=\frac{g_{m2}}{2\pi C_{gs2}}$

* CIRCUIT PARAMETERS ARE DEFINED IN FIGURE 1

larger than the input impedance of the second FET with a low-impedance second-gate termination. The assumption is valid above *X*-band for devices having a gate length of longer than 0.5 μm.

Based on these matrices, the equivalent circuit is simplified to a circuit similar to that of a single-gate FET (see Fig. 2). The input impedance of the dual-gate FET, Z_{in}, is given by

$$Z_{in}\simeq\frac{v_{g1}}{i_{g1}}\simeq R_{g1}+R_{s1}+R_{i1}+(1+R_{s1}g_{m1})/j\omega C_{gs1}. \quad (4)$$

Here, ω is angular frequency and the circuit parameters are as defined in Fig. 1. It is seen that the input impedance is comparable to that of a single-gate FET.

The output impedance Z_{out} can be obtained by using Thevenin's theorem:

$$Z_{out}\simeq 1\Big/\left[Y_{d2}-\frac{Y_{mg2}Y_{md2}}{Y_{g2}+Y_{d1}}+j\omega C_f\right]. \quad (5)$$

Combining (5) and Table I, the capacitance and the resistance for the parallel equivalent circuit (see Fig. 2) are obtained:

$$C_{out}\simeq C_{ds}+C_{dg2}+C_{ds2}/(1+B_2^2)+C_{gs2}/\left[(1+B_2^{-2})g_{m2}R_{ds2}\right]+C_f \quad (6a)$$

$$R_{out}\simeq(1+B_2^2)R_{ds2}/F_b \quad (6b)$$

where B_2 is defined by

$$B_2=f_{T2}/f=g_{m2}/\omega C_{gs2} \quad (7a)$$

and F_b is the positive feedback term for the common gate stage defined by

$$F_b=1-g_{m2}R_{ds2}C_{ds2}/C_{gs2}. \quad (7b)$$

Equations (6) show that the output capacitance is larger than that of a comparable single-gate device due to the larger number of parasitic capacitances involved and the extra capacitance induced by the second gate. The output shunt resistance is also larger and decreases as the frequency increases.

The transconductance of the dual-gate FET is given by

$$G_{md}\simeq-\frac{Y_{md2}Y_{md1}}{Y_{g2}+Y_{d1}}\frac{j\omega C_{gs1}}{Y_{g1}}. \quad (8a)$$

Equation (8a) can be further simplified:

$$G_{md}\simeq g_{m1}/(1+j/B_2). \quad (8b)$$

G_{md} decreases as frequency increases. This is attributed to the capacitive shunting effect of the second gate; as frequency increases, a part of the RF current generated at the virtual drain of the first FET flows through the second FET gate, resulting in reduced G_{md}.

The unilateral gain G_u of the dual-gate FET is given by

$$G_u=\frac{|Y_{21}-Y_{12}|^2}{4[\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22})-\mathrm{Re}(Y_{12})\mathrm{Re}(Y_{21})]} \quad (9)$$

where Re denotes the real part of a complex number. Combining (9) and Table I, G_u becomes

$$G_u\simeq G_{us}B_2^2/F_b \quad (10)$$

with

$$G_{us}\simeq\frac{1}{4}B_1\left(\frac{R_{ds1}}{R_{g1}+R_{s1}+R_{i1}}\right) \quad (11a)$$

$$B_1=f_{T1}/f=g_{m1}/\omega C_{gs1}. \quad (11b)$$

Here, G_{us} is the unilateral gain of a comparable single-gate FET. It is interesting to note that the unilateral gain of the dual-gate FET drops 12 dB/octave at high frequency in contrast to the 6-dB/octave gain roll-off for a single-gate FET or for a dual-gate FET at low frequency. The gain roll-off is the result of the frequency dependent reductions in the output resistance and the transconductance (see (6) and (8)).

The stability factor k of a dual-gate FET is given by

$$k=\frac{2\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22})-\mathrm{Re}(Y_{12}Y_{21})}{|Y_{12}\cdot Y_{21}|}. \quad (12)$$

In terms of the equivalent circuit parameters, (12) can be rewritten as

$$k\simeq(k)_{\mathrm{single}}F_b\Big/\left[B_2\left|\frac{Z_{in2}}{Z_{out2}}+(1-jB_2)\frac{C_f}{C_{dg1}}\right|\right] \quad (13)$$

where $(k)_{\mathrm{single}}$ is the k factor of a single-gate FET and is given by

$$(k)_{\mathrm{single}}\simeq\frac{2|Z_{in1}|}{(R_{s1}+R_{g1}+R_{i1})R_{ds2}g_{m1}(C_{dg1}/C_{gs1})}. \quad (14)$$

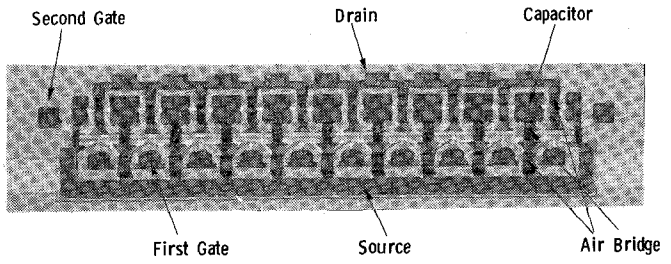

Fig. 3. Photograph of a dual-π-gate FET (gatewidth = 1200 μm).

In (13), it is assumed that $k > 2$. It is seen that the stability factor of a dual-gate FET is larger than that of a single-gate FET when the denominator of (13) is smaller than F_b. A higher stability can be achieved when the two parasitic capacitors C_{ds2} and C_f are small. If the two capacitors are large, the dual-gate FET can be very unstable. Also, it is worth noting that as the common gate stage positive feedback term F_b increases, the output resistance increases and so does the unilateral gain of the dual-gate FET, but only at the expense of the stability.

The reverse transmittance of a dual-gate FET is given by

$$Y_{12} \simeq (Y_{12})_{\text{single}} \frac{Z_{\text{in2}}}{Z_{\text{out2}}(1 - jB_2)} + j\omega C_f \qquad (15)$$

where $(Y_{12})_{\text{single}}$ is Y_{12} of a single-gate FET ($\sim j\omega C_{dg1}$). The reverse transmittance is smaller than that of a single-gate FET as long as C_f is smaller than C_{dg1}, as is usually the case.

The maximum stable gain is obtained as

$$MSG = \left|\frac{Y_{21}}{Y_{12}}\right| \simeq \left|\frac{Y_{md1}Y_{md2}}{Y_{mg1}Y_{mg2} + j\omega C_f Y_{g2}}\right|$$
$$\simeq \left| B_1 B_2 Y_{g1} \Big/ \left[j\omega C_f (1 - jB_2) + \left(j\omega C_{dg2} + \frac{R_{s1} Y_{g1}}{Z_{\text{out1}}} \right) / Z_{\text{out2}} \right] \right|. \qquad (16)$$

Equation (16) shows that the maximum stable gain is the cascaded gain of the two stages when C_f is near zero. However, the denominator of (16) is very small and so a small parasitic capacitor C_f can reduce the gain drastically.

III. Design and Performance of a Dual-Gate Power FET

The high-frequency device model as discussed above was used to design a dual-gate power FET for variable output power applications up to K-band. Specifically, a monolithic MIM capacitor was used for the second-gate termination to minimize the phase shift as the gain is varied and to have stable operation. Due to the excellent high-frequency performance of the pi-gate structure [13], it was adopted for the dual-gate implementation. Fig. 3 shows a 1.2-mm gatewidth FET with a monolithic silicon nitride MIM capacitor connecting between the second gate and the source for each 120 μm of gatewidth. These capacitors are located on the second-gate pads between the drain pads and are grounded to the source with air bridges. The capacitor has a nominal value of ~1.3 pF for each 120 μm of gatewidth.

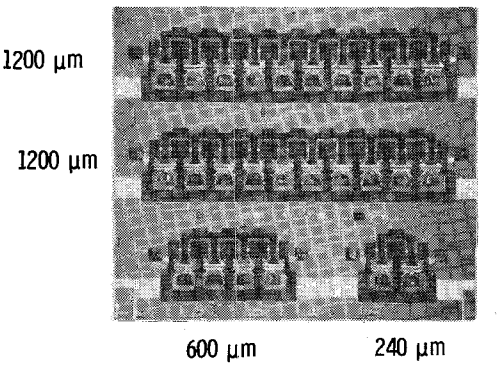

Fig. 4. π-gate structure dual-gate FET's.

TABLE II
20 GHz GaAs Dual-Gate Power FET Design Parameters

EPITAXIAL DOPING LEVEL	2.0 - 2.5 x 10^{17} cm^{-3}
SOURCE-DRAIN SPACING	7.5 μm
GATE LENGTH	0.5 μm
GATE WIDTHS	0.24 - 0.48 - 1.2 mm
GATE FINGER WIDTH	60 μm
I_{DSS}	330 mA/mm
V_P	3 - 4 V

The device fabrication is similar to that reported elsewhere [12], [13]. The GaAs active layers are produced by vapor phase epitaxy. The source and drain ohmic contacts are alloyed AuGe/Ni with a 7-μm separation. Ti/Pt/Au gates are defined by electron-beam lithography and have a nominal length of 0.5 μm. FET's with gatewidths of 240 μm, 480 μm, and 1200 μm have been incorporated into a single mask set (see Fig. 4) for tailoring the output power requirements of amplifiers. The device design parameters are summarized in Table II.

The microwave performance of a 1.2-mm device is shown in Table III. At 10 GHz, an output power of 1.1 W with 10.5-dB gain was obtained with a power-added efficiency of 31 percent. The bias conditions were: $V_d = 12$ V, $V_{g1} = -1$ V, and $V_{g2} = 2.5$ V. The output power is slightly higher than that of TI's single-gate FET with comparable gatewidth. However, the power gain is significantly higher (~ 4 to 5 dB). At 3.5 GHz, the device had about the same output power, but with higher gain (14 dB) and higher power-added efficiency (40 percent) at a drain voltage of 10 V. Above X-band, the output power continues to decrease. The same device delivered 340 mW with 5.3-dB gain at 20 GHz. The reduced output power can be explained by the capacitive shunting effects of the second gate as shown in (8b). In large signal levels, the effects reduce the current handling capability of a dual-gate power FET.

The gain control capability of the dual-gate FET at K-band was also investigated. The gain as a function of the second-gate bias voltage for a 1.2-mm dual-gate FET was

TABLE III
OUTPUT POWER AND GAIN VERSUS FREQUENCY
(GATEWIDTH = 1200 μm)

Frequency (GHz)	Input (dBm)	Output (dBm)	Gain (dB)
10	20	30.5	10.5
12	20	29.6	9.6
15	20	27.6	7.6
18	20	26.4	6.4
20	20	25.3	5.3

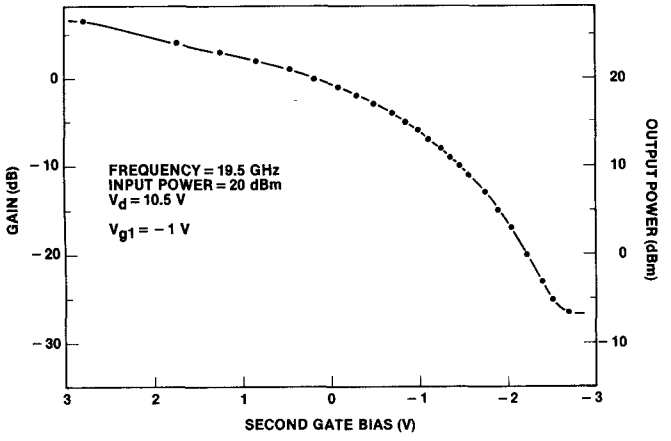

Fig. 5. Gain control of power dual-gate FET (gatewidth = 1200 μm).

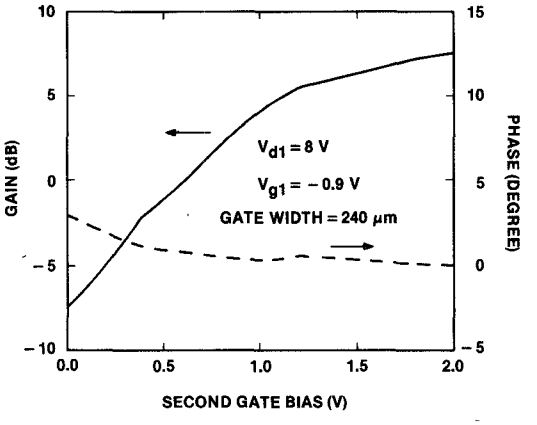

Fig. 7. Gain control and insertion phase change of dual-gate FET at 19 GHz. Input power = 1 mW.

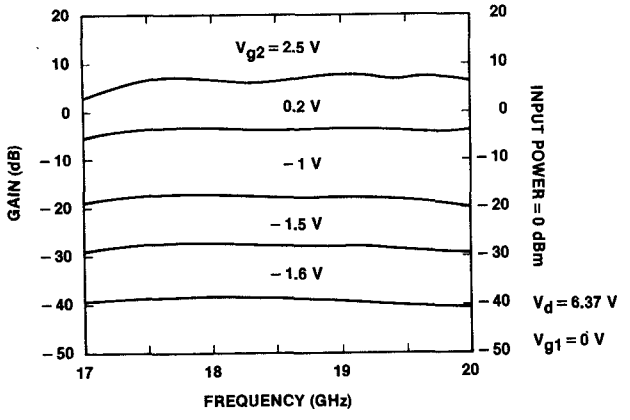

Fig. 6. Gain control of a 240-μm dual-gate FET amplifier across the 18–20-GHz band.

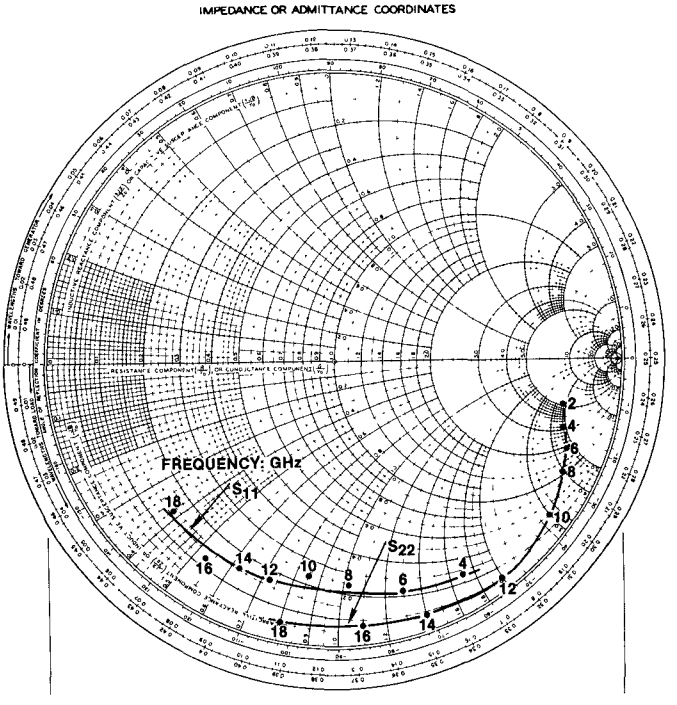

Fig. 8. S_{11} and S_{22} of a 240-μm dual-gate FET.

measured and is shown in Fig. 5. At 19.5 GHz, the gain was varied from 5.6 dB to −27 dB (loss), by changing the second-gate bias from +2.7 V to −2.7 V. The dynamic gain control range is 32.6 dB. The maximum output power was 360 mW with 5.6-dB gain. The gain control of a 240-μm dual-gate FET amplifier (at an input signal level of 1 mW) was also measured. A dynamic gain control range of ~ 45 dB over the 17–20-GHz band has been achieved with a second-gate bias change of from 1.5 V to −1.6 V. Fig. 6 shows the gain (attenuation) versus frequency response with the second-gate voltage as a parameter. The gain shape remains the same across the control range shown. The insertion phase variations of the 240-μm amplifier as a function of the gain control states were also measured. The insertion phase changes no more than ±2 degrees over a 10-dB range (8-dB gain to 2-dB loss) across the same frequency band. Fig. 7 shows the gain control and insertion phase change at 19 GHz.

For the purpose of amplifier design, *S*-parameters of various size FET's were measured over the 2–18-GHz frequency range using an HP automatic network analyzer. Fig. 8 shows a typical Smith Chart plot of the input and

TABLE IV
INPUT (SERIES) AND OUTPUT (PARALLEL) EQUIVALENT CIRCUIT PARAMETERS (GATEWIDTH = 240 μm)

DEVICE	FREQUENCY	INPUT		OUTPUT	
	(GHz)	R_i	C_i	R_{out}	C_{out}
SINGLE-GATE	-	10	0.35	320	0.07
DUAL-GATE	10	11	0.37	1200	0.12
	12	9	0.38	1100	0.14
	14	8	0.37	1000	0.16
	16	8	0.4	670	0.18
	18	8	0.45	500	0.22
				RESISTANCE: Ω	
				CAPACITANCE: pF	

output impedances of a 240-μm gatewidth FET. The series equivalent input impedance and the parallel equivalent output impedance as obtained from the chart and computer-fitted over the 10–18-GHz range are shown in Table IV. For the purpose of comparison, the pertinent impedance data for TI's single-gate FET are also shown. It is obvious from this table that the S_{11} is similar to that of a single-gate FET, but the output resistance and capacitance are much higher than those of a single-gate FET. The output resistance decreases as frequency increases, while the output capacitance increases only slightly. These experimental results follow the theoretical prediction based on the model described in this paper.

IV. Conclusion

A high-frequency equivalent circuit model of a GaAs dual-gate FET and analytical expressions for the input/output impedances, transconductance, unilateral gain, and stability factor are discussed in this paper. It is shown that the unilateral gain of a dual-gate FET rolls off ~12 dB/octave in contrast to the 6-dB/octave roll-off of a single-gate FET or a dual-gate FET at low frequencies. The faster gain roll-off is due to the combined effects of the decreased output resistance and transconductance as the frequency increases. Because of the inherent reduced reverse transmittance, the dual-gate FET can be more stable than the single-gate FET. However, it is shown that certain parasitic elements, such as the input/output feedthrough capacitance and the source–drain capacitance of the second FET, can render the dual-gate FET more unstable than a single-gate FET. For a stable amplifier operation, it is essential that minimization of these parasitic elements should be taken into consideration in selecting a particular device design. In addition to the high-frequency device modeling, a dual-gate power FET suitable for variable gain amplifier applications up to *K*-band has been designed, fabricated, and characterized. At 10 GHz, a 1.2-mm gatewidth device has achieved an output power of 1.1 W with 10.5-dB gain and 31-percent power-added efficiency. The power gain is significantly higher (4–5 dB) than that of a single-gate FET of the same gatewidth. At 3.5 GHz, the same device has achieved the same output power but at a higher gain (14 dB) and power-added efficiency (40 percent). At 20 GHz, an output power of 340 mW with 5.3-dB gain was obtained. The rapid drop in power and gain were also predicted by the analysis discussed in this paper. The gain control capability versus the insertion phase variations was also measured. At 19.5 GHz, a dynamic gain control range of 32.6 dB with a maximum output power of up to 360 mW was obtained. For a broad-band amplifier, a dynamic gain control range of ~ 45 dB over the 17–20-GHz band has been achieved. The insertion phase changed no more than ± 2 degrees over the first 10 dB of gain control. These devices are being implemented in a multistage variable power amplifier for an array antenna in satellite communication applications.

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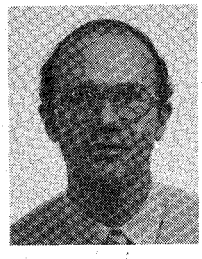

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Design of Broad-Band Power GaAs FET Amplifiers

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Abstract—**A model is presented for the drain–gate breakdown phenomenon of GaAs FET's, based on experimental results. This breakdown model is added to a previously published large-signal model and incorporated in a powerful computer-aided design program called** LSFET. **The program is capable of searching for the optimum power load for an FET and simulating the power performance of multistage amplifiers. The design of power amplifiers is discussed in detail, using the knowledge gained from** LSFET. **Data is presented from a fabricated monolithic broad-band power amplifier chip showing good agreement between measured results and simulated curves.**

I. INTRODUCTION

REQUIREMENTS to design an amplifier with the best gain and power performance in a wide frequency band necessitate a different approach and technology from the design of narrow-band amplifiers. First, a large-signal FET model has to be developed in order to predict the power saturation correctly. This model should not require a time-consuming data-taking technique as in the load-pull method, but still has to be comprehensive and capable of generating large-signal parameters under any bias voltage, RF signal levels, and any load conditions. Secondly, it is important to have an understanding of the interaction between the circuits and FET's in order to realize the best compromise between the gain, power, ripple, and bandwidths. Few papers have discussed these problems previously.

Some studies have been published on large-signal models of GaAs FET's, in which the nonlinear behavior of g_m and G_d, as well as the forward gate current, were discussed [1]–[3]. However, the gate breakdown was never modeled based on experimental data, though it is considered one of the important power-limiting mechanisms of FET's. We will first describe the experimental results of the breakdown phenomenon and then discuss its implementation in the large-signal model described in the previous paper [1].

In the next section, we will demonstrate the application of this large-signal model to a broad-band power amplifier design. A CAD program that simulates and predicts the

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